REMARKS

Claims 1-16 are pending in this application. Claims 17 and 18 have been canceled and claims 13-16 have been amended in this Amendment.

Regarding the Drawings

A Request for Approval of Drawing Changes has been filed herewith to label Fig. 14 as "Prior Art".

Claims 13 and 14 are objected to.

The objection is overcome by the amendments to claims 13 and 14. The amendments delete the references in these claims to claims 1 and 2, respectively, and insert the corresponding limitations on the electrode structure.

Claims 15 and 16 are rejected under 35 U.S.C. 112, second paragraph.

The rejection is overcome by the amendments to the claims. Claims 15 has been amended to depend only from claim 13 and claim 16 has been amended to depend only from claim 14.

Claims 1-16 are rejected under 35 USC 103(a) as being unpatentable over applicant's cited Kazue (JP 11-68253) in view of Takemura (JP 4-98841), and further in view of Misawa (US 6,150,725).

The rejection of claims 1-16 is respectively traversed.

The Examiner asserts that Kazue discloses an electrode structure where a conductive film (metallic film 13) is formed on a substrate through an insulating film (polyimide layer 12). The Examiner admits that Kazue does not disclose a plurality of poles as recited in the claims.

The Examiner asserts that Takemura discloses two dielectrics that are disposed as poles.

The Examiner asserts that Misawa discloses a hard layer 120 and an insulating polyimide layer 121.

Applicants respectively submit, however, that Takemura does not disclose poles. A polysilicon film 20 of Takemura is buried in a trench 18 (see attached sheet with marked up English abstract of this reference). The polysilicon film 20 of Takemura is not buried in holes, but rather deposited to fill trench 19. Thus, the polysilicon 20 of Takemura does not comprise a pole.

Therefore, Takemura, Kazue and Misawa neither teach nor suggest poles, and no *prima facie* case of obviousness can be made for the claims using these references.

According to the present invention, since the film of a high hardness is formed on the side surfaces of the poles of polyimide, the poles are prevented from peeling off, even when a strong force is applied upon the bonding pad. According to the present invention, since the thick polyimide layer is formed below the bonding pads, a parasitic capacity between the bonding pads and the lower layer can be small, whereby radio-frequency signals can be used.

Kazue, Takemura and Misawa neither teach or suggest the technique of the present invention.

As described above, it would have been unobvious to one of ordinary skill in the art at the time the invention was made have applied the teachings of Kazue in view of Takemura, and further view of Misawa.

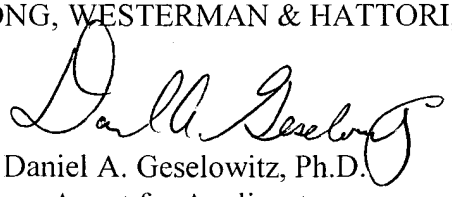
A marked-up version showing the changes made by the present amendment is attached hereto as "Version with Markings to Show Changes Made."

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned agent at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP



Daniel A. Geselowitz, Ph.D.
Agent for Applicants
Reg. No. 42,573

Atty. Docket No. **991387**
Suite 1000
1725 K Street, N.W.
Washington, D.C. 20006
Tel: (202) 659-2930
DAG/plb
Enclosures: Version with Markings to Show Changes Made
Marked-up English Abstract of JP4-98841(A)
H:\FLOATERS\DAG\Amendments\991387.amendment filed 1.24.02.frm

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please amend claims 13 - 16 as follows:

13. (Amended) A semiconductor light-emitting device including a waveguide, a lower electrode formed below the waveguide, and an upper electrode formed above the waveguide,

the upper electrode having an electrode structure ~~according to claim 1,~~

the electrode structure including a conductive film formed on a base substrate through an insulation film, the insulation film comprising a plurality of poles of polyimide, a first film formed on side surfaces of the poles and formed of an insulation material having a higher hardness than polyimide, and a second film of polyimide buried among said a plurality of poles with the first film formed on the side surfaces thereof.

14. (Amended) A semiconductor light-emitting device including a waveguide, a lower electrode formed below the waveguide, and an upper electrode formed above the waveguide,

the upper electrode having an electrode structure ~~according to claim 2,~~

the electrode structure including a conductive film formed on a base substrate through an insulation film,

the insulation film comprising a first film of polyimide having a plurality of openings a first film of polyimide having a plurality of openings which reach the base substrate, a second film formed on inside walls of the openings and formed of an insulation material having a higher hardness than polyimide, and a plurality of poles of polyimide buried in the openings with the second film

formed on the inside walls thereof.

15. (Amended) A semiconductor light-emitting device according to claim 13, further comprising

a high resistance layer formed on a side of the waveguide; and

~~an~~ said electrode structure ~~according to claim 1~~ formed on the high resistance layer.

16. (Amended) A semiconductor light-emitting device according to claim 14, further comprising

a high resistance layer formed on a side of the waveguide; and

~~an~~ said electrode structure ~~according to claim 2~~ formed on the high resistance layer.

(54) SEMICONDUCTOR DEVICE
(11) 4-98841 (A) (43) 31.3.1992 (19) JP
(21) Appl. No. 2-216635 (22) 17.8.1990
(71) IWATSU ELECTRIC CO LTD (72) MITSUHARU TAKEMURA(1)
(51) Int. Cl[5]. H01L21/60,H01L21/76

PURPOSE: To suppress the spreading components in the lateral direction of P-N junction capacitance between buried layers and first semiconductor layers and to lessen the capacitance between an electrode pad and the rear of a semiconductor substance by a method wherein dielectric which are extended from the buried layers to the first semiconductor layers in the longitudinal direction are provided in such a way that the buried and first semiconductor layers in the vicinity of the arrangement region of the electrode pad are respectively isolated from the buried and first semiconductor layers on the peripheries of the buried and first semiconductor layers in the vicinity of the region where pads are provided.

CONSTITUTION: A resist 16 and parts, which are located in openings 17, of a silicon oxide film 14 are removed, an etching, which penetrates an N-type silicon epitaxial layer 13 and a buried layer 12 and reaches a P-type silicon semiconductor layer 11, is performed and trenches 18 are formed. Then, polysilicon films 20 which are dielectrics are deposited in such a way that the trenches 18 are completely filled and after that, the polysilicon films 20 are etched to the position of the firstly formed film 14 and the surfaces of the polysilicon films 20 are made flat. Moreover, a field oxidation is performed to make thick the film 14 and a circuit element is formed. After that, an electrode pad 21 for wire bonding use is formed on the film 14. Thereby, the capacitance between the pad 21 and the rear of a semiconductor substrate can be lessened.